REMARKS

As a preliminary matter, Applicants have cancelled claims 4 and 5, without prejudice.

As another preliminary matter, Applicants have amended the preamble of the independent claims to clearly define that the present invention relates to "reading recorded data from a recording medium having an address part for recording an address and a data part for recording data in that the data part has a higher recording density than the address part."

Claims 1, 4 and 5 stand rejected over Shimada et al. (U.S. Patent No. 5,056,116) in view of Byrne et al. (U.S. Patent No. 6,487,672), and further in view of Sprague (U.S. Patent No. 6,072,645). Claims 2, 6-8, 12-13 stand rejected over the references as applied to claims 1, 4 and 5, and also in view of Leung et al. (U.S. Patent No. 6,564,518). Claims 9-11 stand rejected over the same references applied to claims 1, 4 and 5, and also in view of Bushy, Jr. (U.S. Patent No. 4,896,337) and further in view of Scheffler (U.S. Patent No. 5,041,921)). Further, claims 14-17 stand rejected over the references as applied to claims 1, 4 and 5, and further in view of Bushy, Jr., Scheffler, and Leung.

Applicants traverse all of the rejections of all the claims because the cited references do not disclose or suggest an apparatus with a first clock signal generating part and a second clock signal generating part for the address, and a third clock signal generating part and a fourth clock signal generating part for the data, as in the amended independent claims. In particular, the amended claims recite, in relevant part:

"a first clock signal generating part generating a first clock signal;

a second clock signal generating part generating a second clock signal faster than the first clock signal;

a third clock signal generating part generating a third clock signal;

a fourth clock signal generating part generating a fourth clock signal faster than the third clock signal;

a sampling part sampling a read signal from recorded data of a recording medium by synchronizing with the first clock signal when the recorded data is the address recorded in the address part and by synchronizing with the third clock signal when the recorded data is the data in the data part;

a first storing part consecutively storing a sample value obtained by said sampling part; and

a data detecting part retrieving the sample value from said first storing part by synchronizing the second clock signal when the sample value is sampled from the address recorded in the address part and by synchronizing the fourth clock signal when the sample value is sampled from the data recorded in the data part, and detecting data by processing the sample value in accordance with a predetermined algorithm,"

The references do not disclose or suggest the present invention as recited. More particularly, the references do not disclose or suggest an apparatus that includes four clock signal generating parts, the first and the second being for the address recorded in the address part, and the third and the fourth being for data recorded in the data part, wherein the second is faster than the first, and the fourth is faster than the third. Referring to FIGs. 3 and 4, two clock signals for sampling are associated with the PLL 17, and two clock signals for detection are associated with the synthesizer 32/47. The purpose of this structure is for generating different clock signals to correspond to different recording densities (the data part

has a higher recording density than the address part, as recited in the amended preamble). The four clock signals enable the read system and the detection system to operate independently of one another.

Shimada does not disclose these features because Shimada does not disclose four clock signal generating parts. Shimada merely discloses a process clock, CLK1, which is used as a sampling clock, and a process clock for sampling, CLK2, which has a half frequency of the process clock CLK1. The CLK2 of Shimada is merely associated with the digital phase locked loop circuit 11, the rate converter circuit 13, and the data decoding circuit 14, which operate based on the processing clock CLK2 (col. 19, lines 30-40, FIG. 22). The CLK2 of Shimada is not associated with a data detecting part (FIG. 22). Further, Shimada is not directed to a read system and a detection system that can be independently operated, as in the present invention. Further still, Shimada is not directed to a read system and detection system having four clock signal generating parts to correspond to different recording densities. Thus, Shimada does not disclose or suggest the features of all amended independent claims 1, 12, 13, 14 and 16.

Byrne does not remedy the deficiencies of Shimada. Byrne merely discloses a configuration to supply adjusted sampling data to a detector.

Sprague does not remedy the deficiencies of Byrne and Shimada, and is merely directed to a recording device, such as an audio tape recorder, in which the recent past is temporarily recorded in a memory until the user can select a retroactive start time to record the data onto a medium. In the retroactive recording device of Sprague, past information is

temporarily stored in a solid state retroactive memory, and based on a selection of buttons by the user, such as "START A," "START B," AND "START C," the retroactive recording device transfers the past information to the audio tape. Since the retroactive recording device of Sprague is a recording device, and not a device to read data from a recording medium, even if the data demodulation apparatus of Shimada and the retroactive recording device of Sprague are combined, features of the present invention cannot be achieved.

Further, each additional reference does not remedy the deficiencies of Shimada, Byrne and Sprague, but are cited for a particular additional feature in each claim. Applicants submit that none of these references taken alone or in combination, disclose or suggest the invention as claimed.

Leung is merely cited for disclosing "an apparatus data detecting part having a recursive process conducting part conducting a recursive process for the sample data retrieved from the first storing part in accordance with the predetermined algorithm so that maximum likelihood data is detected." However, Leung is a detector error suppression circuit that is used to remove single bit errors by comparing samples to detected EPR4 bits.

Bushy is cited for disclosing an apparatus that has two different memory devices that receive data and that switch between the memory devices. However, Bushy merely discloses a configuration to adjust the frequency of successive data, the configuration utilizing two memories, an input memory and an output memory. The input memory receives input data at a high frequency, while simultaneously the output memory outputs the stored data at a low frequency. In the present application, however, the sampling data is written in

to the FIFO memory and the sampling data is read out from the FIFO memory to be used for recursive detection. One FIFO memory stores the MO data and another FIFO memory stores the ID.

Scheffler is cited for teaching a second storing part that consecutively stores a sample value obtained by a sampling part. Scheffler is merely directed to a system for recording custom albums from a library of pre-recorded items.

Zook is cited for disclosing the feature of storing address data. However, Zook is merely directed to an error correction apparatus that corrects an error burst occurring in the header information such as the sector ID data.

Neither the primary references Shimada, Byrne nor Sprague, and additionally Leung et al., Zook, Bushy and Scheffler, disclose the structure of the present invention as recited. More particularly, the references do not disclose or suggest an apparatus that includes four clock signal generating parts, the first and the second being for the address recorded in the address part, and the third and the fourth being for data recorded in the data part, wherein the second is faster than the first, and the fourth is faster than the third.

It is submitted that the question under 35 U.S.C. §103 is whether the totality of the art would collectively suggest the claimed invention to one of ordinary skill in this art. The test is whether the invention as a whole, in light of all of the teachings of the references in their entireties, would have been obvious to one of ordinary skill in the art at the time the invention was made. It is insufficient that the art disclosed components of Applicants' invention, either separately or used in other combinations. A teaching, suggestion, or

incentive must exist to make the combination made by Applicants. In this case, there is no incentive in the references to combine. Moreover, even if, arguendo, such an incentive existed, the combination of references would not result in an apparatus as claimed in all independent claims 1, 12, 13, 14 and 16. Accordingly, Applicants submit the rejections of all the claims have been overcome and should be withdrawn.

For all of the above reasons, Applicants request reconsideration and allowance of the claimed invention. Should the Examiner be of the opinion that a telephone conference would aid in the prosecution of the application, or that outstanding issues exist, the Examiner is invited to contact the undersigned.

Respectfully submitted,

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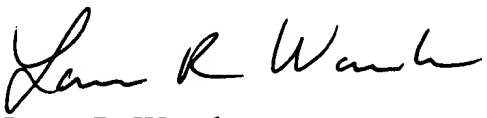
By 

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